Fig 1

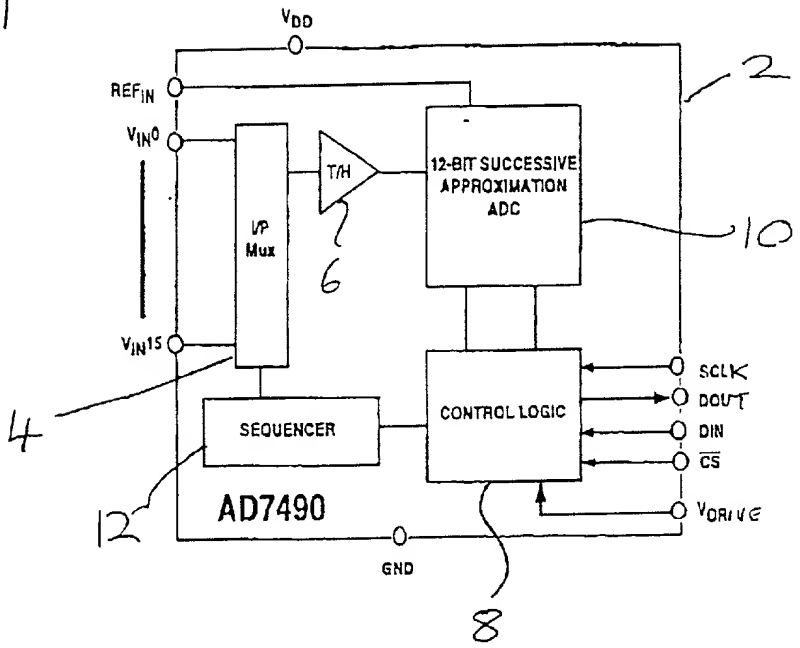
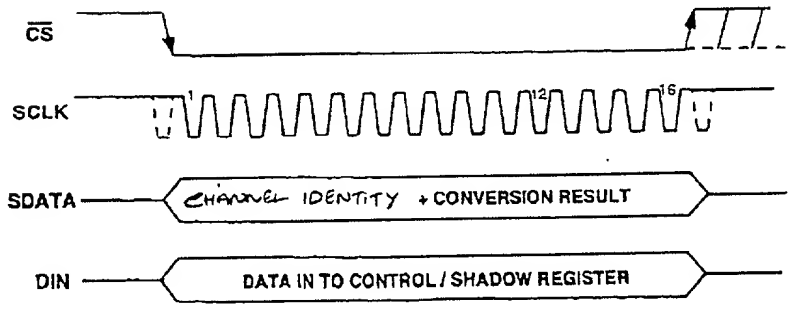


Fig 8



CONTROL REGISTER DATA IS LOADED IN ON FIRST 12 SCLK CYCLES.
SHADOW REGISTER DATA IS LOADED IN ON FIRST 16 SCLK CYCLES

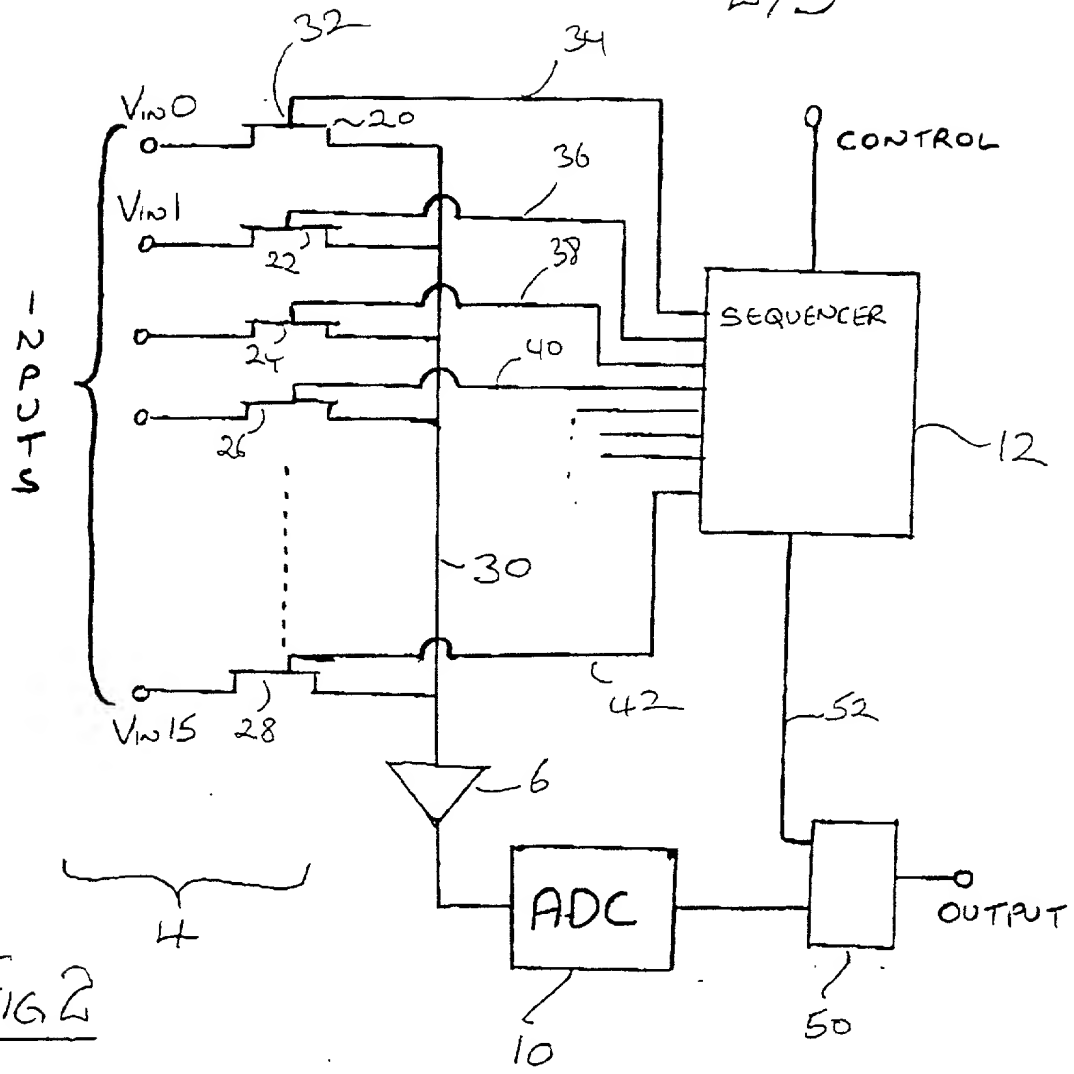


FIG 2

MSB											LSB
WRITE	SEQ	ADD3	ADD2	ADD1	ADD0	PM1	PM0	SHADOW	WEAK/$\overline{TRI}$	RANGE	CODING

FIG 6

MSB															LSB
$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$	$V_{IN}8$	$V_{IN}9$	$V_{IN}10$	$V_{IN}11$	$V_{IN}12$	$V_{IN}13$	$V_{IN}14$	$V_{IN}15$
S0	S1	S2	S3	S4	. . . .										S15

FIG 7

Fig 3

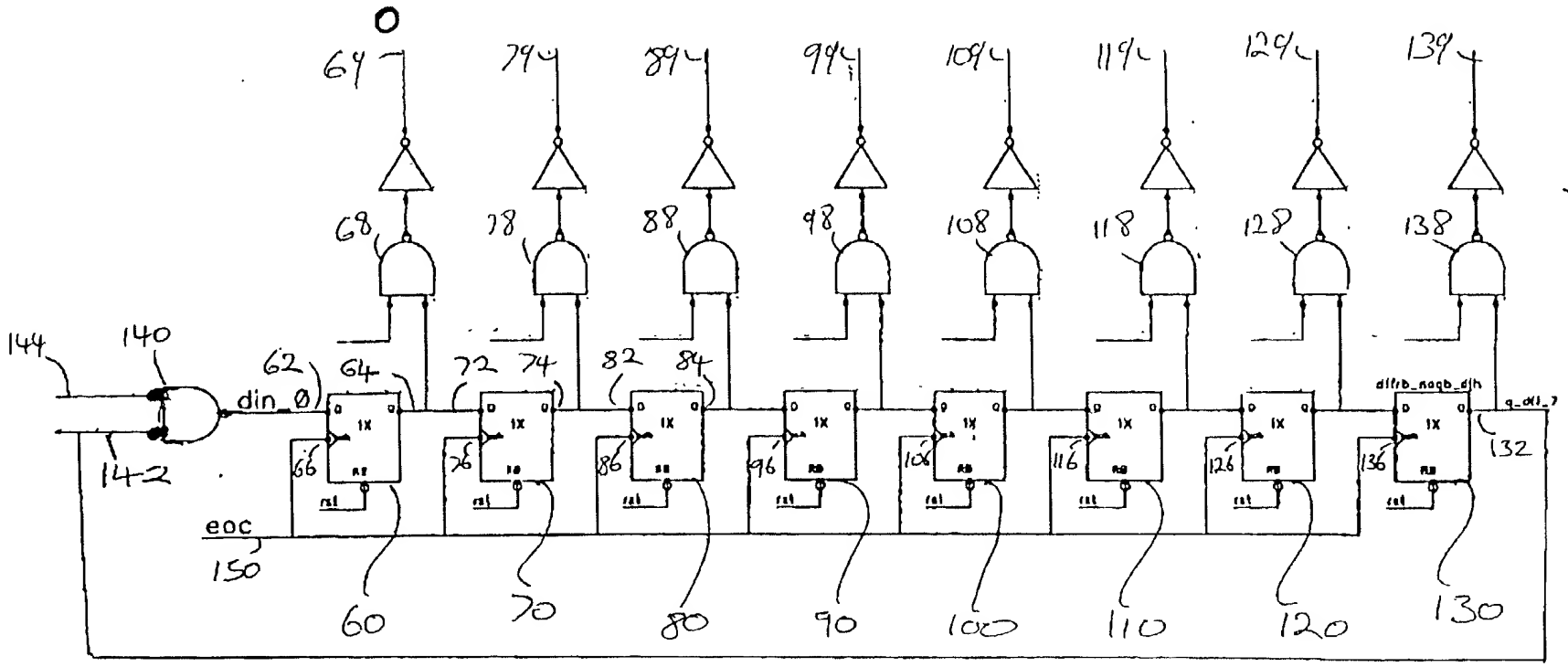
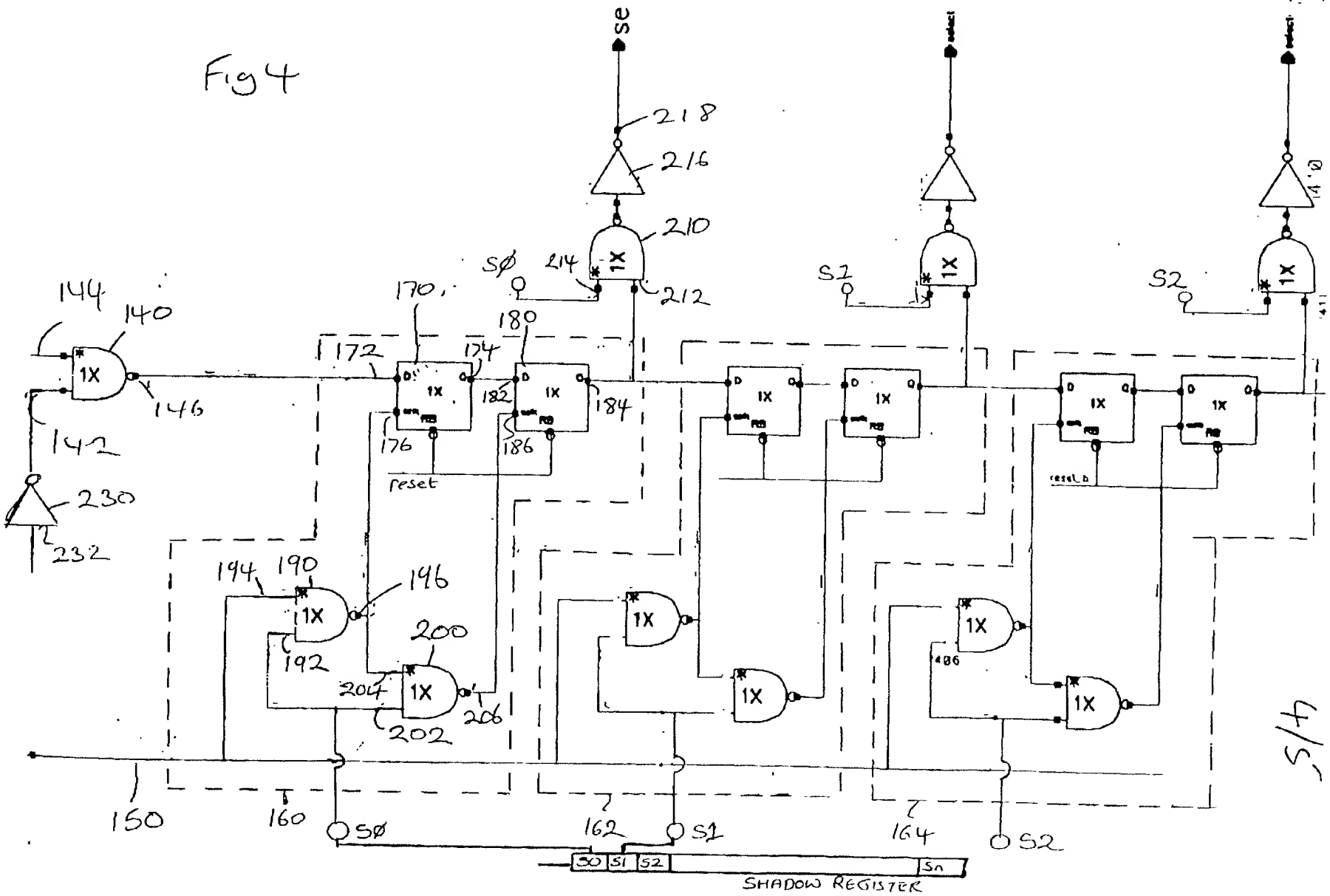

64
74
84
94
104
114
124
134
68
78
88
98
108
118
128
138
144
140
62
64
72
74
82
84
din_0
142
eoc
150
66
76
86
96
106
116
126
136
132
60
70
80
90
100
110
120
130

Fig 4


se
218
216
210
214
212
SØ
S1
S2
144
140
146
142
230
232
170
172
174
180
182
184
176
186
reset
194
190
196
192
200
204
202
206
150
160
162
164
SØ
S1
S2
SHADOW REGISTER
S0
S1
S2
Sn
1X

4/5

Fig 5